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(71) Applicant (for all designated States except US): NUMERICAL TECHNOLOGIES, INC. [US/US]; Suite 207, 333 West Maude Avenue, Sunnyvale, CA 94086 (US).			
(72) Inventors; and (75) Inventors/Applicants (for US only): WANG, Yao-Ting [-/US]; 970 Corte Madera Avenue #311, Sunnyvale, CA 94086 (US). PATI, Yagyensh, C. [US/US]; 1199 Cleveland Street, Redwood City, CA 94061 (US).			
(54) Title: PHASE SHIFTING CIRCUIT MANUFACTURE METHOD AND APPARATUS			
(57) Abstract A method and apparatus for creating a phase shifting mask and a structure mask for shrinking integrated circuit designs. One embodiment of the invention includes using a two mask process. The first mask is a phase shift mask and the second mask is a single phase structure mask. The phase shift mask primarily defines regions requiring phase shifting. The single phase structure mask primarily defines regions not requiring phase shifting. The single phase structure mask also prevents the erasure of the phase shifting regions and prevents the creation of undesirable artifact regions that would otherwise be created by the phase shift mask. Both masks are derived from a set of masks used in a larger minimum dimension process technology.			

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PHASE SHIFTING CIRCUIT MANUFACTURE METHOD AND APPARATUS

1. Related Applications

5 This application relates to, claims benefit of the filing date of, and incorporates by reference, the United States provisional patent application entitled, "Transistor Manufacturing Using Phase Shifting," having serial number 60/025,972, and filed September 18, 1996, and which is assigned to the assignee of the present invention.

2. The Background of the Invention

a. The Field of the Invention

10 This invention relates to the field of integrated circuit manufacturing. In particular, the invention relates to phase shifting techniques in the optical lithography patterning process.

15

b. Background Information

Lithography processing is a required and essential technology when manufacturing conventional integrated circuits. Many lithography techniques exist, and all lithography techniques are used for the purpose of defining geometries, features, lines, or shapes onto an integrated circuit die or wafer. In general, a radiation sensitive material, such as photoresist, is coated over a top surface of a die or wafer to selectively allow for the formation of the desired geometries, features, lines, or shapes.

20 One known method of lithography is optical lithography. The optical lithography process generally begins with the formation of a photoresist layer on the top surface of a semiconductor wafer. A mask having fully light non-transmissive opaque regions, which are usually formed of chrome, and fully

light transmissive clear regions, which are usually formed of quartz, is then positioned over the aforementioned photoresist coated wafer. Light is then shone on the mask via a visible light source or an ultra-violet light source. In almost all cases, the light is reduced and focused via an optical lens system which contains one or several lenses, filters, and or mirrors. This light passes through the clear regions of the mask and exposes the underlying photoresist layer, and is blocked by the opaque regions of the mask, leaving that underlying portion of the photoresist layer unexposed. The exposed photoresist layer is then developed, typically through chemical removal of the exposed/non-exposed regions of the photoresist layer. The end result is a semiconductor wafer coated with a photoresist layer exhibiting a desired pattern. This pattern can then be used for etching underlying regions of the wafer.

In recent years, there has been great demand to increase the number of transistors on a given size wafer. Meeting this demand has meant that integrated circuit designers have had to design circuits with smaller minimum dimensions. However, prior to the work of Levenson, et. al., as reported in "Improving Resolution in Photolithography with a Phase Shifting Mask," IEEE Transactions on Electron Devices, VOL., ED-29, Nov. 12, December 1982, pp. 1828-1836, it was found that the traditional optical lithography process placed real limits on the minimum realizable dimension due to diffraction effects. For, at integrated circuit design feature sizes of 0.5 microns or less, the best resolution has demanded a maximum obtainable numerical aperture (NA) of the lens systems. However, as the depth of field of the lens system is inversely proportional to the NA, and since the surface of the integrated circuit could not be optically flat, good focus could not be obtained when good resolution was obtained and vice versa. Thus, as the minimum realizable dimension is reduced in manufacturing processes for semiconductors, the limits of optical lithography technology are being reached. In particular, as the minimum dimension approaches 0.1 microns, traditional optical lithography techniques will not work

effectively.

One technique, described by Levenson, et. al., to realize smaller minimum device dimensions, is called phase shifting. In phase shifting, the destructive interference caused by two adjacent clear areas in an optical lithography mask is used to create an unexposed area on the photoresist layer. This is accomplished by making use of the fact that light passing through a mask's clear regions exhibits a wave characteristic such that the phase of the amplitude of the light exiting from the mask material is a function of the distance the light travels in the mask material. This distance is equal to the thickness of the mask material. By placing two clear areas adjacent to each other on a mask, one of thickness t_1 and the other of thickness t_2 , one can obtain a desired unexposed area on the photoresist layer through interference. For, by making the thickness t_2 such that $(n-1)(t_2)$ is exactly equal to $1/2 \lambda$, where λ is the wavelength of the light shone through the mask material, and n is the refractive index of the material of thickness t_1 , the amplitude of the light exiting the material of thickness t_2 will be 180 degrees out of phase with the light exiting the material of thickness t_1 . Since the photoresist material is responsive to the intensity of the light, and the opposite phases of light cancel where they overlap, a dark unexposed area will be formed on the photoresist layer at the point where the two clear regions of differing thicknesses are adjacent.

Phase shifting masks are well known and have been employed in various configurations as set out by B.J. Lin in the article, "Phase-Shifting Masks Gain an Edge," *Circuits and Devices*, March 1993, pp. 28-35. The configuration described above has been called alternating phase shift masking (APSM). In comparing the various phase shifting configurations, researchers have shown that the APSM method can achieve dimension resolution of 0.25 microns and below.

One problem with the APSM method is that dark lines on the photoresist layer are created at all areas corresponding to 0 degree to 180 degree transitions

in the mask. These dark lines, unless part of the desired end structure, should be erased at some point in the processing of the wafer.

Another problem is that the APSM method does not lend itself well to process technology shrinking. Traditionally, designers design an integrated circuit for a predetermined minimum realizable dimension. However, because process technologies can require a considerable amount of time to fine tune, the integrated circuit is first manufactured using a process technology that does not support the designed for speed and has a larger minimum dimension. Often, a first set of masks are created to manufacture the integrated circuits at the larger dimension. As the process technology improves, the minimum realizable dimension decreases. Additional mask sets are created for each new minimum dimension process. These masks are generally created using software driven machines to automatically manufacture the masks given the design features needed. However, due to the complexity of the masks needed to erase the aforementioned unwanted dark lines created when the APSM method is used, these masks have not generally been able to be designed automatically by mask creation programs. This has required mask designers to expend large amounts of time and money manually creating mask layouts when the APSM method is used.

Spence, U.S. Patent Number 5,573,890, reveals one method to overcome these problems. Spence discloses a system in which phase shifting is used to shrink integrated circuit design, specifically to shrink transistor gate lengths, where the masks used are computer designed. The computer designs a mask or masks which achieve(s) the required minimum dimension and which provide for the removal of the unwanted dark lines created by the APSM method. In a disclosed single mask method, Spence uses transition regions to compensate for the unwanted dark lines that would have been produced where there were 0 degree to 180 degree transitions in the mask. The problem with this single mask method is that the single mask that results is complicated and difficult to

manufacture. Further, the mask that is produced is very unlike the design of the circuit from a visual standpoint, thus making it difficult for designers to visually double check their work.

Spence also discloses a two mask method which is illustrated in Figure 1.

5 Old mask 100 represents a typical mask that would be used to produce a structure having a transistor of old gate length 109, which is wide enough to be achieved using traditional optical lithography techniques with no phase shifting. New gate length 159 is the desired transistor gate length that is smaller than the smallest dimension realizable through the process of traditional optical
10 lithography. Spence uses a phase shift and structure mask 110 and a trim mask 120 in order to achieve the new gate length 159 and to remove the unwanted dark lines created by the phase shift method, respectively.

The phase shift and structure mask 110 is designed such that it contains both a structure chrome area 113, which is the same shape as the desired polysilicon
15 structure of the circuit, and a phase shifter consisting of a 180 degree phase clear area 112 adjacent to a 0 degree phase clear area 111. When light is shined on the phase shift and structure mask 110, the phase shift and structure image 130 is created on the underlying photoresist layer. The phase shift and structure image 130 contains the desired final structure dark area 133 and the desired dark
20 area 132, but also includes unwanted artifacts 135 created by interference at the transitions between the 180 degree phase clear area 112 and the 0 degree phase clear area 111.

Thus, in order to remove these unwanted artifacts 135 and achieve the desired result image 150, Spence discloses using the trim mask 120 solely to
25 perform this function. The trim mask 120 consists of a chrome area 123 and an erasure light area 122. When light is shown on the trim mask 120, the trim image 140 is created on the photoresist layer. This trim image 140 contains an erasure light area 142 which serves to erase the unwanted artifacts 135. The result image 150 represents the final image created on the photoresist layer as a

result of the two mask method disclosed by Spence.

Spence's two mask method has several problems. By combining the production of the final structure and the phase shifting onto a single mask, this method introduces a large number of possible conflicts in the design rules of the circuit as a whole. This increase in conflicts makes it much more difficult for the computer to determine a solution to the shrinking of the circuit design that is within the design rules parameters. In addition, this increase in conflicts may in some instances produce a situation where no shrunk design is possible. Furthermore, combining the structure and phase shifting on one of the two masks increases the overall complexity of this mask thus making it more difficult to manufacture and inspect. Finally, combining structure and phase shifting on a single mask results in the design of a mask that does not look like the structure masks used for the earlier larger versions of the designed circuit. As a result, it is more difficult for the designers of the integrated circuit to visually check their work.

Therefore, what is desired is an improved method of using phase shifting to achieve smaller minimum realizable dimensions.

3. A Summary of the Invention

A method and apparatus for creating a phase shifting mask and a structure mask for shrinking integrated circuit designs is described.

One embodiment of the invention includes using a two mask process. The first mask is a phase shift mask and the second mask is a single phase structure mask. The phase shift mask primarily defines regions requiring phase shifting. The single phase structure mask primarily defines regions not requiring phase shifting. The single phase structure mask also prevents the erasure of the phase shifting regions and prevents the creation of undesirable artifact regions that would otherwise be created by the phase shift mask. Both masks are derived from a set of masks used in a larger minimum dimension process technology.

Although many details have been included in the description and the figures, the invention is defined by the scope of the claims. Only limitations found in those claims apply to the invention.

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4. A Brief Description of the Drawings

The figures illustrate the invention by way of example, and not limitation. Like references indicate similar elements.

Figure 1 illustrates a prior art dual mask phase shifting process.

10 Figure 2 illustrates one embodiment of a dual mask phase shifting process for shrinking transistor gates in an integrated circuit.

Figure 3 illustrates one embodiment of a dual mask phase shifting process for shrinking an integrated circuit design.

Figure 4 illustrates one embodiment of a method of creating the masks found in Figures 2 and 3.

15 Figure 5 illustrates one embodiment of a desired integrated circuit structure and effective design rules.

Although many details have been included in the description and the figures, the invention is defined by the scope of the claims. Only limitations found in those claims apply to the invention.

20

5. The Description

a. An Overview of an Embodiment of the Invention

25 A method and apparatus for creating a phase shift mask and a structure mask for shrinking integrated circuit designs is described. One embodiment of the invention includes using a two mask process. The first mask is a phase shift mask and the second mask is a single phase structure mask. The phase shift mask primarily defines regions requiring phase shifting. The single phase structure mask primarily defines regions not requiring phase shifting. The single phase structure mask also prevents the erasure of the phase shift regions

and prevents the creation of undesirable artifact regions that would otherwise be created by the phase shift mask. Both masks are derived from a set of masks used in a larger minimum dimension process technology.

5 The following describes the use of a technique, in one embodiment of the invention, to shrink a design of a polysilicon layer for use in a transistor. The design is shrunk from a first process technology that does not use phase shifting to a second process technology that does use phase shifting. A phase shift mask, for the polysilicon layer, is created solely to make the gate of the transistor; the width of the gate is the minimum distance for the second process technology.

10 This phase shift mask does not contain any of the structural elements of the remainder of the circuit. The semiconductor substrate is exposed using the first mask. A structure mask is created to make the remainder of the layer of the integrated circuit and to protect the desired phase shift regions. The semiconductor substrate is also exposed using this second mask. The first mask

15 and the second mask are generated directly from the information used to generate the mask set for the first process technology.

In one embodiment, the second mask is exactly the same mask as was used in the first process technology. In another embodiment, the second mask has the same pattern used for the first process technology except that the dimensions

20 used have been shrunk. In another embodiment, the second mask used has a similar pattern to the mask used for the first process technology except that a few modifications to the pattern have been made.

b. Gate Width Shrinking

25 Figure 2 illustrates one embodiment of a dual mask phase shifting process for shrinking transistor gates in an integrated circuit. The following paragraphs first describe the elements in Figure 2, then the relationships between those elements, and then the functions of the various elements of the system.

Figure 2 includes the following elements: An old mask 100, a phase shift

mask 210, a structure mask 220, a phase shift mask image 230, a structure mask image 240, and a result image 250. The old mask 100 includes a clear area 101, a gate chrome area 102, a structure chrome area 103, and an old gate length 109. The phase shift mask 210 includes a 180 phase clear area 213, a 0 phase clear area 215, phase shift mask chrome 216, and control chrome 217. The structure mask 220 includes variable gate protect chrome 222, a clear area 224, and structure chrome 226. The phase shift mask image 230 includes a gate dark area 232, a phase shift mask light area 233, and an other dark area 236. The structure mask image 240 includes a gate protect dark area 242, a structure light area 244, and a structure dark area 246. The result image 250 includes a light area 251, a gate dark area 232, a structure dark area 246, and a new gate length 259.

The following paragraphs describe the general relationships between the elements and the main elements of Figure 2. Old mask 100 is the same as in Figure 1.

Phase shift mask 210 represents a top view of a mask used solely to produce a desired circuit dimension that requires the use of interference, such as a shrunk transistor gate length. The 180 degree phase clear area 213 is situated adjacent to the 0 degree phase clear area 215, and each of these clear areas is designed to allow for the full transmission of light through it. The 180 degree phase clear area 213 is of a thickness such that it will create destructive interference at its boundary with the 0 degree phase clear area 215. The control chrome 217 is opaque and does not allow for the transmission of light through it. The control chrome 217 is placed over the center of the boundary between the 180 degree phase clear area 213 and the 0 degree phase clear area 215. The width of this control chrome 217 is variable and can be completely excluded. The width of the control chrome 217 is used to control the shrunk gate length. The phase shift mask chrome 216 covers the remainder of the mask and is also opaque. The sole purpose of the phase shift mask chrome 216 is to ensure the remainder

of the photoresist layer is left unexposed such that a structure may later be imprinted on the photoresist layer by the structure mask 220.

Structure mask 220 represents a top view of a mask used to imprint the desired polysilicon structure on the photoresist layer. The structure mask 220 also protects the transistor gate formed by the phase shift mask 210, and erases any unwanted artifacts created by the phase shift mask 210. The clear area 224 is designed to allow the full transmission of light through it, and is designed to cover any areas where unwanted artifacts may have been formed by the phase shift mask 210. The structure chrome 226 is opaque and is shaped and sized to define the desired polysilicon circuit structure. The variable gate protect chrome 222 is of a variable width designed to cover the entire area that the desired gate might occupy in order to protect the gate from inadvertent exposure.

Phase shift mask image 230 represents a top view of a photoresist coated silicon wafer after the wafer has had light shined on it while phase shift mask 210 was directly over the wafer. The light areas depict regions where the photoresist layer was exposed to the light.

Structure mask image 240 represents a top view of a photoresist coated silicon wafer after the wafer has had light shined on it while structure mask 220 was directly over the wafer. The light areas depict regions where the photoresist layer was exposed to the light.

Result image 250 represents the top view of a photoresist coated silicon wafer that has had light shined on it on two separate occasions. Once with phase shift mask 210 directly over the wafer, and once with structure mask 220 directly over the wafer. For the purposes of this invention, it does not matter what sequence is used. Either mask can be used first with no effect on the result image 250.

The following paragraphs describe the function of the elements of Figure 2. When old mask 100 is placed over a photoresist coated silicon wafer and light is

shined onto the mask, the light is transmitted through the clear area 101, and the photoresist material underlying the clear area 101 is exposed. Similarly, the light shined onto the mask is not transmitted through the opaque gate chrome area 102, or the opaque structure chrome area 103, and the photoresist material underlying these areas is thus not exposed. The exposed photoresist layer is now ready for development, typically by chemically removing the exposed regions of the photoresist layer. The end result would be a large dimension semiconductor wafer coated with a photoresist layer exhibiting the desired pattern of transistor gate width and polysilicon structure.

When phase shift mask 210 is placed over a photoresist coated silicon wafer and light is shined onto the mask, the light is transmitted through the 0 degree phase clear area 215 and the 180 degree phase clear area 213. This results in the underlying photoresist material being exposed and creating the phase shift mask light area 233 displayed as part of phase shift mask image 230. The light does not transmit through the phase shift mask chrome 216 and thus the underlying photoresist is not exposed resulting in the other dark area 236 of the phase shift mask image 230. At the boundary between the 180 degree phase clear area 213 and the 0 degree phase clear area 215, destructive interference occurs and the photoresist underlying this boundary is not exposed resulting in the production of the gate dark area 232. The light does not transmit through the control chrome 217 and thus the underlying photoresist is not exposed. The width of the control chrome 217 is variable and can be varied to change the length of the gate dark area 232. This feature allows for greater control over the width of the gate dark area 232 produced when the design does not require the maximum gate shrinking possible via phase shifting.

When structure mask 220 is placed over a photoresist coated silicon wafer and light is shined onto the mask, the light is transmitted through the clear area 224, and the photoresist material underlying the clear area 224 is exposed. This exposure will erase any unwanted artifacts created by the phase shift mask 210,

and produces the structure light area 244 of structure mask image 240. The light does not transmit through the variable gate protect chrome 222 resulting in the gate protect dark area 242. The variable gate protect chrome 222 is sized such that its width is greater than the desired transistor gate length. This ensures
5 that the gate dark area 232 produced by phase shifting will not be destroyed by inadvertent exposure. The light does not transmit through the structure chrome 226 resulting in the production of the structure dark area 246 which correlates to the shape and size of the desired polysilicon structure.

The advantages of this dual mask phase shifting process are significant, and
10 overcome the problems associated with the process disclosed by Spence. These advantages stem from the fact that, the phase shift mask 210 is used solely to produce a desired circuit dimension that requires the use of interference such as a shrunk transistor gate length, while a second separate structure mask 220 is used to produce the remaining polysilicon structure and erase any unwanted
15 artifacts. First, manufacturing of the masks is greatly simplified in that there is no combination of features on one mask to be concerned with. Similarly, since the only critical performance feature of the phase shift mask 210 is the placement of the 180 degree phase clear areas 213, it is much easier to inspect the masks after they have been manufactured.

The decreased complexity of the phase shift mask when compared to the
20 combined mask disclosed in Spence also reduces the problem of design rule conflicts. As stated earlier, the combining of phase shift and structure elements on a single mask greatly increases the possible number of design rule conflicts that have to be sorted by the computer to come up with a mask design that will
25 implement the desired shrunk circuit. This results in a much more complicated and time consuming process for the computer, and situations where a solution might not exist. The current invention overcomes these problems by separating the elements onto separate masks which greatly reduces the number of possible design conflicts on a single mask.

Lastly, the masks disclosed in Spence differ substantially from the old mask 100. This is a direct result of combining the phase shift and structure functions on one mask. One embodiment of the invention uses a structure mask 220 that appears very similar to the old mask 100. This is an advantage for integrated circuit designers in that they can visually do a double check of the mask design by comparing the structure mask 220 directly to the old mask 100.

In another embodiment of the invention a portion of the polysilicon circuit structure is included on the phase shift mask. Although less desirable than placing all of the structure on the structure mask, this would add flexibility to the process of mask design. For, in a situation where design rules prevent the design of a structure mask which includes all of the structure, it may be possible to include some of the needed structure on the phase shift mask.

c. Design Shrinking

Figure 3 illustrates one embodiment of a dual mask phase shifting process for shrinking an integrated circuit design. The concepts applicable to Figure 2 apply here as well, and as such the following discussion will focus on the differences between Figures 2 and 3.

Figure 2 illustrated an embodiment solely for the shrinking of a circuit dimension that required interference, in the specific case, the gate length of all transistors in a circuit. Figure 3 on the other hand is an embodiment of a process to shrink an entire integrated circuit design structure including the transistor gate lengths. For purposes of illustration of this embodiment, it is assumed that the chosen shrink factor for the circuit decreased only the transistor gate length to a dimension that required phase shifting. The remainder of the circuit is shrunk using conventional optical lithography methods to implement the design shrink. In another embodiment, the dual mask phase shifting may be used to shrink any area requiring interference.

d. Example Flowchart

Figure 4 illustrates one embodiment of a method of creating the mask found in Figures 2 and 3.

5 This embodiment of the method envisions that each block will be performed by a computer. However, this is not required, and the invention is not limited to a method in which each block is performed by a computer. For instance, a human could perform each of the design steps manually.

10 At block 410, a computer reads in data including old mask layout data that is supplied either manually or by reading files (e.g. a GDS-II file) preexisting in the computer. In one embodiment, this data will include a previous large dimension integrated circuit design, a new gate length dimension to be applied to all transistors in the integrated circuit design, and various other design rules needed for the design of the masks. In another embodiment, this data will include a previous large dimension integrated circuit design, a shrink factor
15 dimension to be applied to the entire integrated circuit, and various other design rules needed for the design of the masks. In another embodiment, this data will include a previous large dimension integrated circuit design, a new gate length dimension to be applied to all transistors in the integrated circuit design, a shrink factor dimension to be applied to the remainder of the integrated circuit,
20 and various other design factors needed for the design of the masks. In still another embodiment, this data will include a previous integrated circuit design with shrunk transistor gate lengths, a shrink factor to be applied to the remainder of the integrated circuit, and various other design factors needed for the design of the masks.

25 At block 420, the computer identifies areas on the new circuit design that have dimensions that are too small to be achieved by traditional optical lithography and that can be achieved through the use of destructive interference. As the limits for optical lithography may vary depending upon the application and the physical limits of the particular equipment, the exact quantity of this

interference dimension is variable and may be supplied by the user at block 410 in addition to the other manufacturing process data.

At block 430, the computer creates a phase shift mask design by locating a phase shift area in each place in the circuit where the computer has previously identified there to be a need for an interference dimension. Each phase shift area includes adjacent clear areas that transmit light 180 degrees out of phase with each other, with the boundary between the areas falling where the interference dimension needs to be. This computer produced design data can then be input into a mask manufacturing device that will convert the design data into a physical mask.

At block 440, the computer creates a structure mask design. The computer analyzes the required circuit structure and designs the mask such that opaque areas appear everywhere that a polysilicon structure so requires. The computer will also design the structure mask such that opaque areas appear over each area that was previously determined to require a phase shift area. The width of this gate protect area is variable and sensitive to user input. The computer will also analyze the design to ensure that clear areas appear wherever needed to erase unwanted phase shift artifacts. This computer produced design data can then be input into a mask manufacturing device that will convert the design data into a physical mask. In one embodiment, the computer generates GDS-II data describing the phase shifting mask and the structure mask.

e. Design Rules

Figure 5 illustrates one embodiment of a desired integrated circuit structure and effective design rules. Figure 5 includes the following elements: a desired structure 500, a phase shift mask 210, and a structure mask 220. The desired structure 500 includes a gate area 510, a diffusion area 520, a polysilicon area 530, a poly protect dimension 540, and an extension dimension 550. The phase shift mask 210 includes a 180 degree phase clear area 213, a 0 degree phase

clear area 215, and a phase shift mask overlap area 217. The structure mask 220 includes variable gate protect chrome 222, a clear area 224, structure chrome 226, desired gate length 259, and a gate protect dimension 525.

5 The actual phase shift mask design must take into account possible imperfections in the mask manufacturing process. These imperfections include mask misalignment and double exposure. Desired structure 500 represents the image of a design structure that takes into account the various dimensions that are required to be defined in order to avoid any problems that may be caused by these potential manufacturing imperfections.

10 One embodiment of the invention is designed to shrink transistor gate length. Thus, the mask must be designed such that the gate area 510 of the transistor is shrunk even if the masks are misaligned. To accomplish this, the phase shift areas on the phase shift mask are designed to be of a width that is equal to the width of the diffusion area 520 plus the two extension dimensions
15 550 shown in Figure 5. The extension dimensions are a function of the maximum possible alignment error involved in the physical mask manufacturing process.

It is also required that the polysilicon area 530 be protected from any inadvertent exposure during the process. This is accomplished by providing the
20 poly protect dimension 540 which is a function of the maximum possible alignment error. Thus in the actual mask design, no phase shift mask phase shift area will be of a width that is within the poly protect dimension 540 of any structure on the structure mask.

Phase shift mask 210 is the same as in Figure 2 except that it shows phase
25 shift mask overlap area 217. Here it is shown that the actual 180 degree phase clear area 213 is larger than the adjacent 0 degree phase clear area 215. This extra material is overlapped by the chrome of the mask, and thus the phase shift mask overlap area 217 does not allow light to transmit through. The size of the phase shift mask overlap area 217 is a function of physical manufacturing needs

in putting the mask together.

Lastly, structure mask 220 is the same as in Figure 2 except that it shows gate protect dimension 525 and desired gate length 259. The variable gate protect chrome 222 is designed to be of a width equal to the desired gate length 259 plus two times the gate protect dimension 525. The gate protect dimension is a function of possible mask misalignment. This dimension serves to ensure that the shrunk gate length produced by the phase shift mask is protected from subsequent inadvertent exposure.

10 f. Conclusion

What has been described is a method and apparatus for creating a phase shift mask and a structure mask for shrinking integrated circuit designs. In one embodiment, the phase shift mask is designed to create dark areas on a photoresist coated silicon wafer which correspond to a particular dimension requiring interference, specifically a shrunk transistor gate length. In another embodiment, the phase shift mask is designed to create dark areas on a photoresist coated silicon wafer which correspond to any desired dimension requiring interference. In each of these embodiments, the structure mask is designed to erase unwanted artifacts created by the phase shift mask, and to produce the remainder of the original polysilicon structure. In another embodiment, the phase shift mask is designed to create dark areas on a photoresist coated silicon wafer which correspond to any desired dimension requiring interference, while the structure mask is designed to erase unwanted artifacts, and to produce the remainder of the polysilicon structure in a shrunk form. In another embodiment, the structure mask is modified to compensate for additional design rules of the target technology. For example, allocations for mask misalignments may require that the second mask be modified slightly.

The Claims

What is claimed is

1. A method of generating a set of mask definitions corresponding to a set of masks for fabricating at least a layer of material of a circuit using a first manufacturing process having a first minimum realizable dimension, said
5 method comprising:
 - accessing a first data set defining at least a portion of a layout of said circuit corresponding to said layer, said layout being for a second manufacturing process having a second minimum realizable
10 dimension, said second minimum realizable dimension being greater than said first minimum realizable dimension;
 - identifying a first set of areas in said layout, destructive light interference being used to realize a dimension of a first set of structures in said layer corresponding to areas in the first set of areas;
 - 15 creating a first mask definition defining a set of phase shifting areas for realizing said first set of structures; and,
 - creating a second mask definition defining a second set of areas in said layout, said second set of areas including at least some areas in said layout defining a second set of structures in said layer and not using
20 destructive light interference to be realized, wherein said first mask definition and said second mask definition are included in said set of mask definitions.
2. The method of claim 1 wherein said first mask definition defines a plurality
25 of opaque areas, a plurality of zero degree phase shift clear areas, and a plurality of 180 degree phase shift clear areas, said plurality of zero degree phase shift clear areas being located near said plurality of 180 degree phase shift clear areas to cause destructive light interference to create said first set of structures.

3. The method of claim 1 wherein said first mask definition defines only the set of phase shifting areas.
- 5 4. The method of claim 1 wherein said second mask definition defines said second set of areas as being opaque.
- 10 5. The method of claim 4 wherein said second mask definition defines a third set of areas, said third set of areas corresponding to a set of clear areas in a mask and wherein said clear areas prevent the creation of undesirable artifact structures that would otherwise be created by the set of phase shifting areas.
- 15 6. The method of claim 1 wherein said first mask definition defines a third set of areas, said third set of areas including at least some areas in said layout defining a third set of structures in said layer, said third set of structures not using destructive light interference to be realized.
- 20 7. The method of claim 1 wherein the second mask definition has a substantially similar layout as the portion of layout of said circuit corresponding to said layer.
- 25 8. A set of masks for using in an integrated circuit manufacturing process, said set of masks comprising:
a first mask having primarily phase shifting areas and first opaque areas;
and a second mask having second opaque areas and clear areas, said
second opaque areas for defining a set of structures not requiring phase
shifting for realization and for preventing erasure of structures created
by the first mask, and said clear areas for further defining said set of
structures and for preventing the creation of artifact structures that
would otherwise be created by the first mask.

9. The set of masks of claim 8 wherein the first mask and the second mask are for defining structures in a single layer of the integrated circuit manufacturing process.
- 5 10. The set of masks of claim 9 wherein the single layer includes polysilicon.
11. The set of masks of claim 8 wherein the phase shifting areas include a set of zero degree phase shift areas and 180 degree phase shift areas, each phase shifting area corresponding to at least one zero degree phase shift area and one
- 10 180 degree phase shift area.
12. The set of masks of claim 8 wherein the phase shifting areas also include chrome areas positioned between adjacent zero degree phase shift areas and 180 degree phase shift areas.

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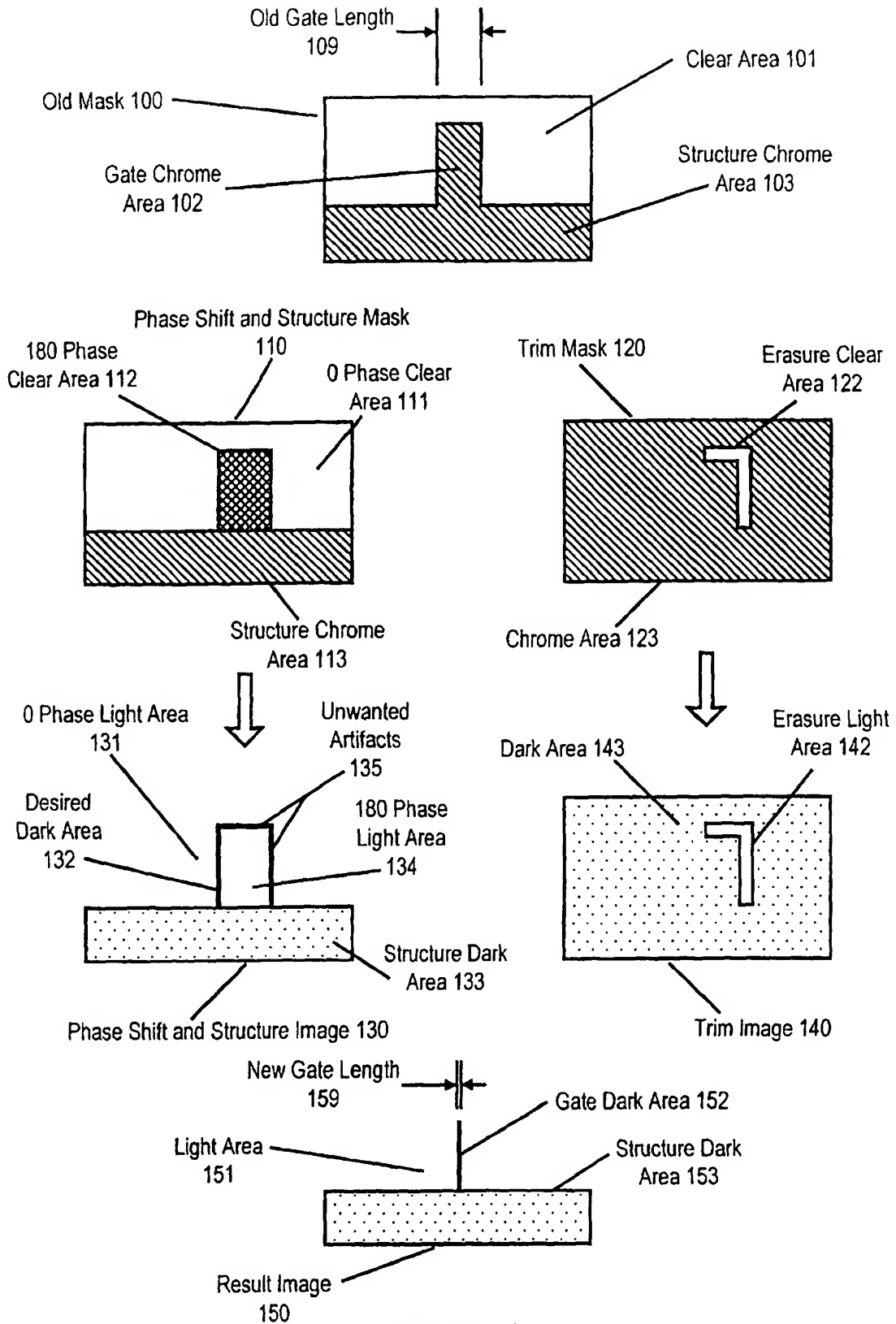


Figure 1
(Prior Art)

SUBSTITUTE SHEET (RULE 26)

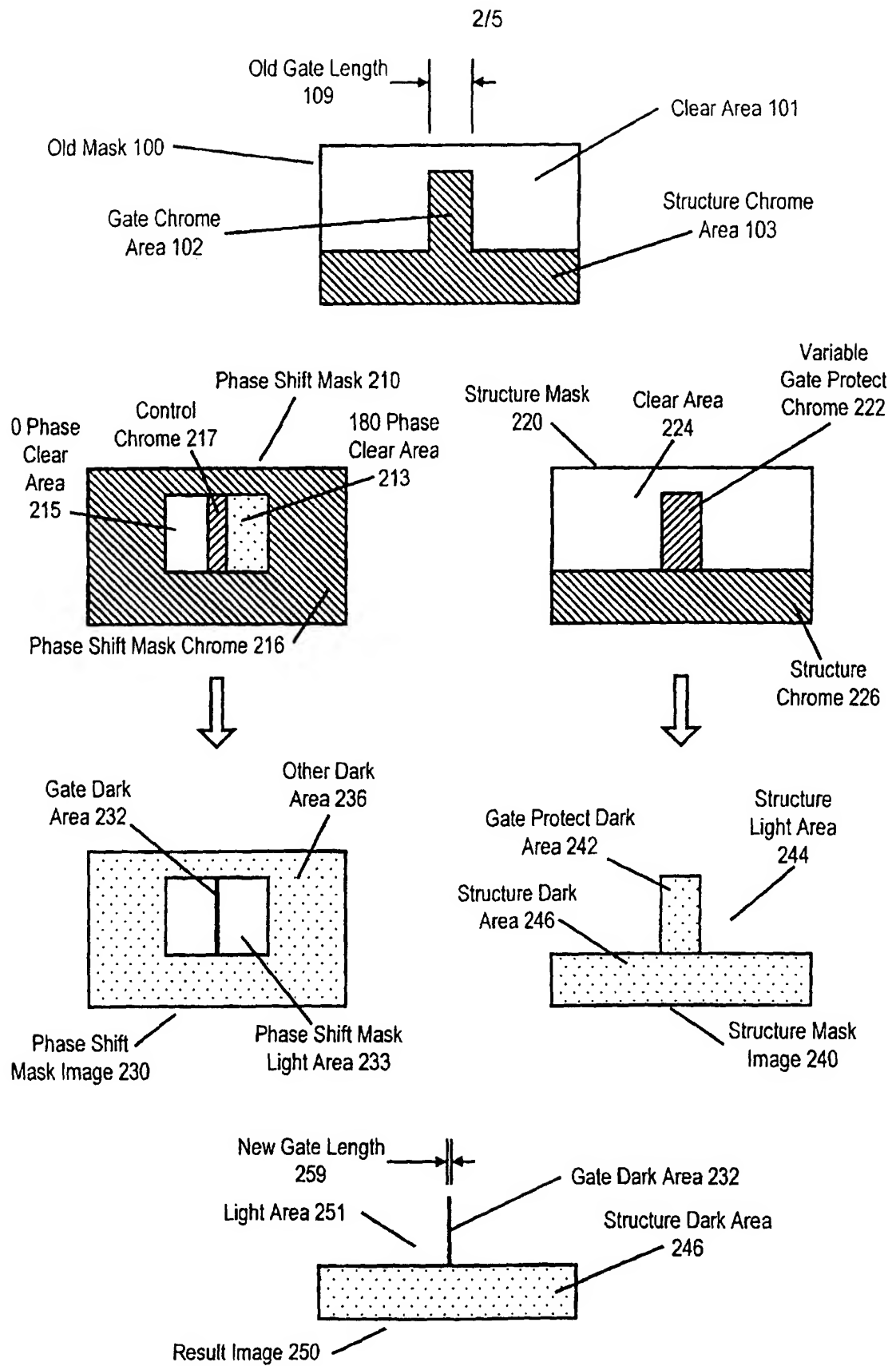


Figure 2

SUBSTITUTE SHEET (RULE 26)

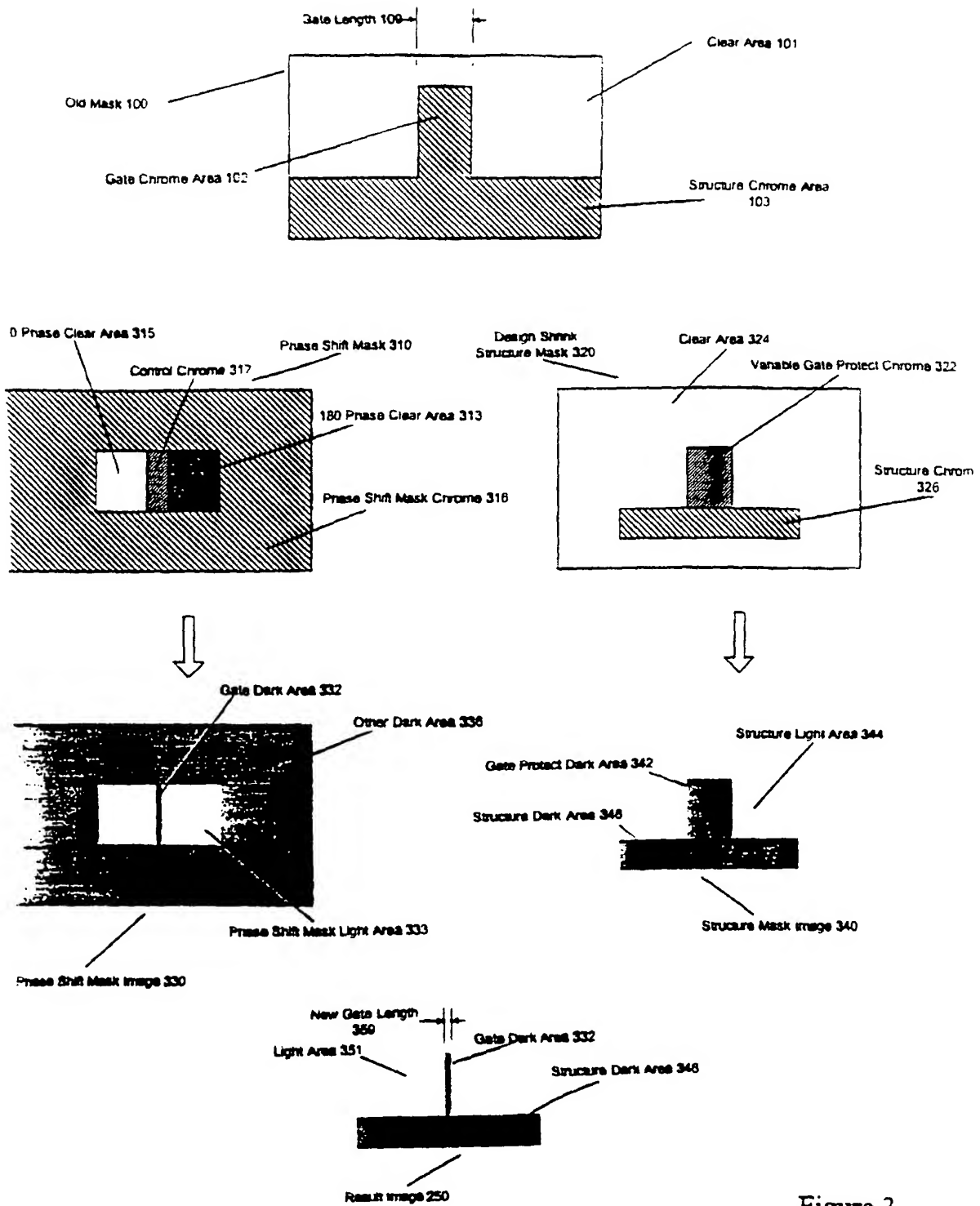
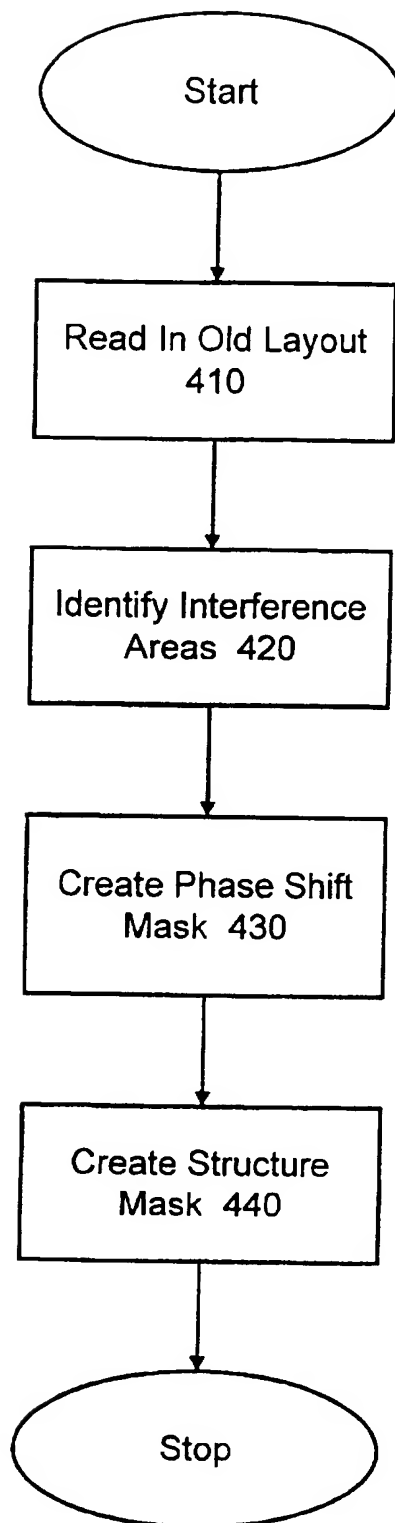
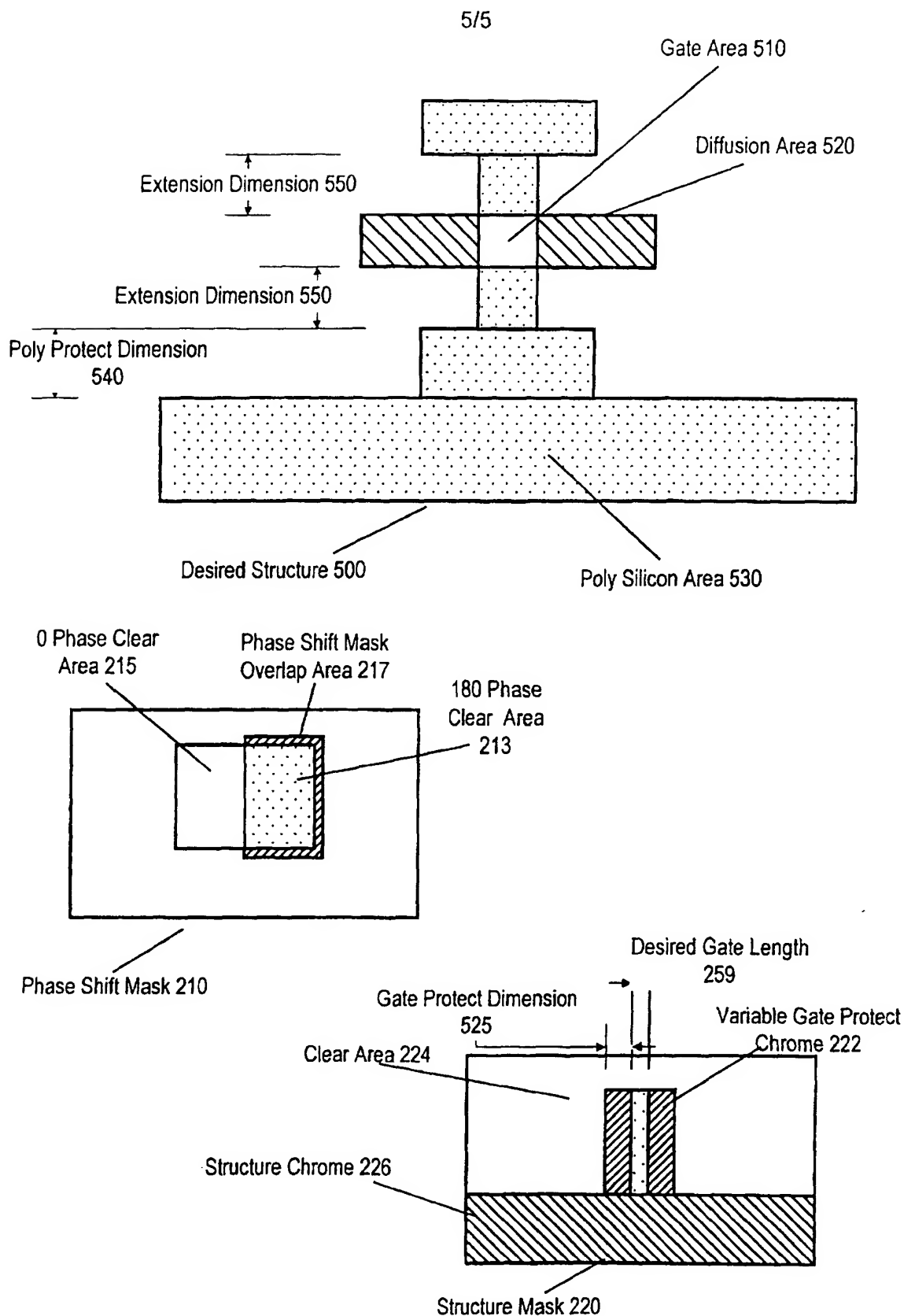


Figure 3

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**Figure 4**

**Figure 5****SUBSTITUTE SHEET (RULE 26)**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/16631

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G03F 9/00

US CL : 430/005, 311, 315, 394

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 430/005, 311, 315, 394

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P --- Y,P	US 5663017A (SCHINELLA ET AL) 02 September 1997, column 9, lines 45-52, column 10 lines 1-50.	8 ----- 1-7, 9-12
X,P --- Y,P	US 5,620,816 A (DAO) 15 April 1997, column 10, lines 37-67.	8 ----- 1-7, 9-12
X --- Y	US 5,364,716 A (NAKAGAWA ET AL) 15 November 1994, column 15, lines 58-68, column 16, lines 1-21.	8 ----- 1-7, 9-12

☐ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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*O"	document referring to an oral disclosure, use, exhibition or other means	*A* document member of the same patent family
*P"	document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

24 OCTOBER 1997

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Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

STEPHEN ROSASCO

Telephone No. (703) 308-0661